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Low Power Adiabatic Logic Design

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Abstract: *Adiabatic describe the thermodynamic processes in which there is no energy exchange with the environment, and therefore very less dissipated energy loss. These circuits are low power circuits which use reversible logic to conserve energy. Adiabatic logic works with the concept of switching activities which reduces the power by giving stored energy back to the supply. The main design changes are focused on power clock which plays the vital role in the principle of operation. This has been used because many adiabaticcircuits use a combined power supply and clock, or a power clock (Four Phase).To achieve this, the power supply of adiabatic logic circuits have used time varying voltage charging signal, in contrast to traditional non-adiabatic systems that have generally used constant voltage charging from a fixed-voltage power supply. Thereby the circuit topology and operation of the circuit has been changed so that the source current of CMOS transistor change its direction and goes back to the supply(Recovery) when the power clock falls from VDD to zero. Power efficient blocks can be designed by using adiabatic logic which can be used in combinational and sequential circuits. The simulation of the designs is done using a backend tool called MENTOR GRAPHICS in 130nm technology.*

Keywords: *Adiabatic Switching, Four Phase Power Clock, Recovery, Thermodynamic Process, Efficient charge recovery logic*

I. Need for Low Power VLSI Design

The ever growing number of transistors integrated on a chip and the increasing transistors switching speed in recent decades has enabled great performance improvement in computer systems by several orders of magnitude. Unfortunately, such phenomenal performance improvements have been accompanied by an increase in power and energy dissipation of the systems. Higher power and energy dissipation in high performance systems require more expensive packing and cooling technologies, increase cost and decreases system reliability.Power dissipation is defined as the rate of energy delivered from source to system/device. Power minimization is one of the primary concerns in today VLSI design methodologies because of the main reasons. One is the long battery operating life requirement of mobile and portable devices and second is due to increasing number of transistors on a single chip leads to higher power dissipation and it can lead to reliability and IC packaging problems. The low power requirements of present electronic systems have challenged the scientific research towards the study of technological, architectural and circuital solutions that allow a reduction of the energy dissipated by an electronic circuit.

One of the main causes of energy dissipation in CMOS circuits is due to the charging and discharging of the node capacitances of the circuits, present both as a load and a parasite. Such part of the total power dissipated by a circuit is called dynamic power. In order to reduce the dynamic power, an alternative approach to the traditional techniques of power consumption reduction, named adiabatic switching has been proposed in the last years. In such approach, the process of charging and discharging the node capacitances is carried in a way so that small amount of energy is wasted and a recovery of the energy stored on the capacitors is achieved.

1.1 Literature Survey

Implementation of circuit in different adiabatic logic, a paper sponsored by IEEE(ICECS 2015)[5], proposed a logic circuit for 4 by 1 multiplexer using efficient charge recovery logic. The power dissipation obtained at 20 MHz frequency is 17.16mW. In this paper we have designed 4 by 1 multiplexer with reduced number of 22 transistors. The power dissipation obtained at 20 MHz frequency in this paper is 320.73uW. The logic implemented hence uses less area and has less power dissipation. ECRL logic implements both true and complemented forms and therefore no extra circuit is required to implement the complemented form

II. Adiabatic Logic

Adiabatic logic is the term given to low-power electronic circuits that implement reversible logic. To increase the energy efficiency of the logic circuits, other measures can be introduced for recycling the energy drawn from the power supply. A novel class of logic circuits called *adiabatic logic*offers the possibility of further reducing energy dissipation during the switching events, and the possibility of recycling, reusing, some

of the energy drawn from the supply. The amount of energy recycling achievable using adiabatic techniques is also determined by fabrication technology, switching speed, and the voltage swing.

2.1 Sources of Power Dissipation

There are three major sources of power dissipation in digital CMOS circuits, each one being affected by different factors and influencing the system in a different way.

2.1.1 Dynamic Power Dissipation

The dominant component of power consumption in a typical CMOS circuits the dynamic switching power. The dynamic switching power is dissipated while charging or discharging the parasitic capacities during the voltage transitions of the nodes within a CMOS circuits. The dynamic switching power is independent of the type of switching gate and the shape of the input wave form (input rise and fall times). The dynamic switching power is dependent only on the supply voltage, the switching frequency, the initial and final voltages, and the equivalent capacitance of a switching note. Since the switching power is independent of the switching gate a block diagram representation of a generic CMOS gate is used to explain dynamic switching power dissipation is CMOS circuits.

2.1.2Short Circuit Power Dissipation

Short circuit power dissipation is due to the direct-path short circuit current I_{se} which arises when both the NMOS and PMOS transistors are simultaneously active, conducting current directly from supply to ground. The expression for short circuit power dissipation is given by: $P_{sc}=I_{SC}.V_{DD}$ Where P_{sc} is the short circuit power dissipation

2.1.3Leakage Power Dissipation

Finally, leakage current I_{le} which can arise from substrate injection and sub threshold effects is primarily determined by fabrication technology considerations. The expression for the leakage power dissipation given by: $P_{le} = I_{le}.V_{DD}$where P_{le} is the leakage power dissipation.

2.2 Adiabatic Switching

Energy-Recovery is also called as adiabatic switching. Adiabatic switching can be achieved by ensuring that the potential across the switching devices is kept arbitrarily small. This can be achieved by charging the capacitor from a time varying voltage source or constant current source. Adiabatic logic circuits thus require non-standard power supplies with time varying voltage, also called pulsed power supplies. Also, the dissipated energy is proportional to R, as opposed to the conventional case, where the dissipation depends on the capacitance and the voltage swing. Thus, reducing the on resistance of the PMOS network will reduce the energy dissipation.

2.3 Adiabatic Logic Families

The adiabatic circuits are divided into two logic families

2.3.1 Fully adiabatic circuits

In fully adiabatic logic, all the charge on the load capacitance is recovered by the power supply. Fully adiabatic logic circuits face a lot of problems with respect to operating speed and input power clock synchronization. Hence we go for the implementation of partially adiabatic circuits.

2.3.2Partially adiabatic circuits

In partially adiabatic logic, some charge is allowed to be transferred to the ground.

2.3.2.1 Efficient Charge Recovery Logic (ECRL)

2.3.2.2 Positive Feedback Adiabatic Logic (PFAL

2.3.2.3 NMOS Energy Recovery Logic (NERL)

2.3.2.4 Clocked Adiabatic Logic (CAL)

2.3.2.5 Source-coupled Adiabatic Logic (SCAL).

Out of all the above logics,efficient charge recovery logic shows better performance in terms of less power dissipation and comparatively less area.

III. Efficient Charge Recovery Logic

Efficient charge recovery logic of an inverter schematic is shown in Fig. 3.1displays cross coupled PMOS transistors. It has the structure similar to Cascade Voltage Switch Logic (CVSL) with differential signaling. ECRL is a low energy adiabatic circuit. It adopts a new method that performs Pre-charge and evaluation simultaneously. It consists of two cross-coupled transistors M1 and M2 and two NMOS transistors in the circuit. An AC power supply is used for ECRL gates, so as to recover and reuse the supplied energy. Both

OUT and OUT1 are generated so that the power clock generator can always drive a constant load capacitance independent of the input signal.

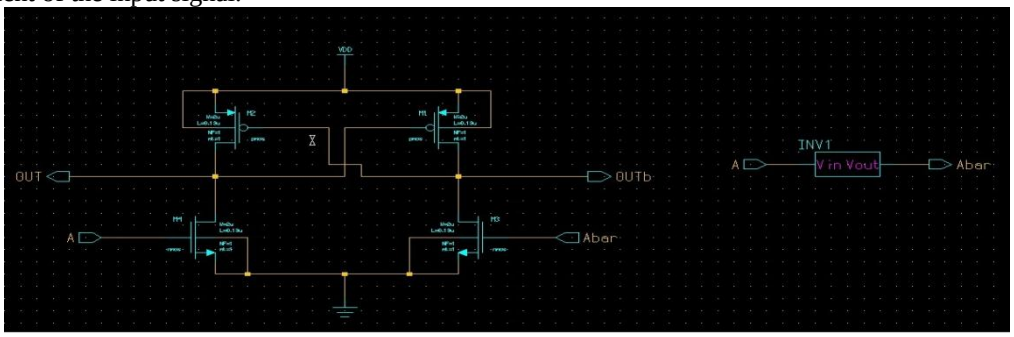

Fig. 3.1 ECRL logic Invertor.

Full Output swing is obtained because of the cross-couple PMOS transistors in the pre charge and recovers phases. But due to the threshold voltage of the PMOS transistors, the circuits suffer from the non-adiabatic loss both in the pre charge and recover phases. That is, to say, ECRL always pumps charge on the output with a full swing. Initially, input IN is high and IN1 is low. When power clock rises zero to VDD, OUT remains ground level. Output OUT1 follows the power clock.When power clock reaches VDD, outputs OUT and OUT1 hold logic value zero and VDD respectively. This output values can be used for the next stage as an inputs. Now power clock falls from VDD to Zero, OUT1 returns its energy to power clock hence delivered charge is recovered. ECRL uses four phase clocking rule to efficiently recover the charge delivered by power clock.

3.2 Simulated Waveform

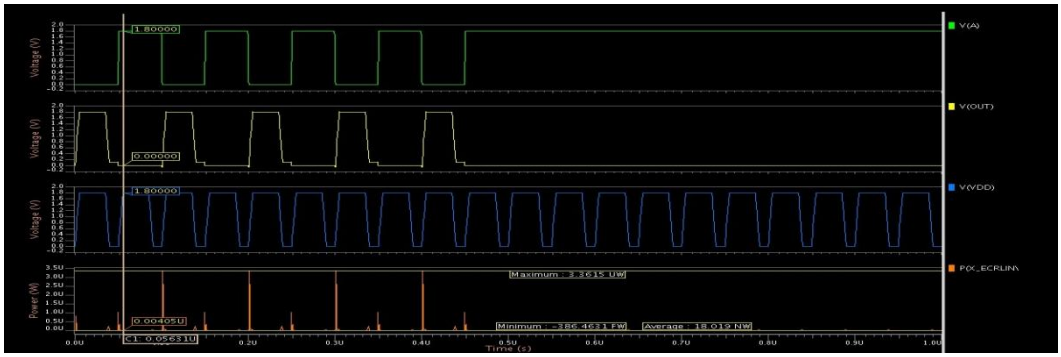

Fig 3 Inverter waveforms

IV. Design Of Three Input Universal Gates

Boolean Expression for 3 input NAND gate is **Q = A.B.C**.It is implemented using ECRL logic with cross coupled PMOS transistors for recovery logic from node capacitances.

4.1 Three Input Nand Ecrl Schematic

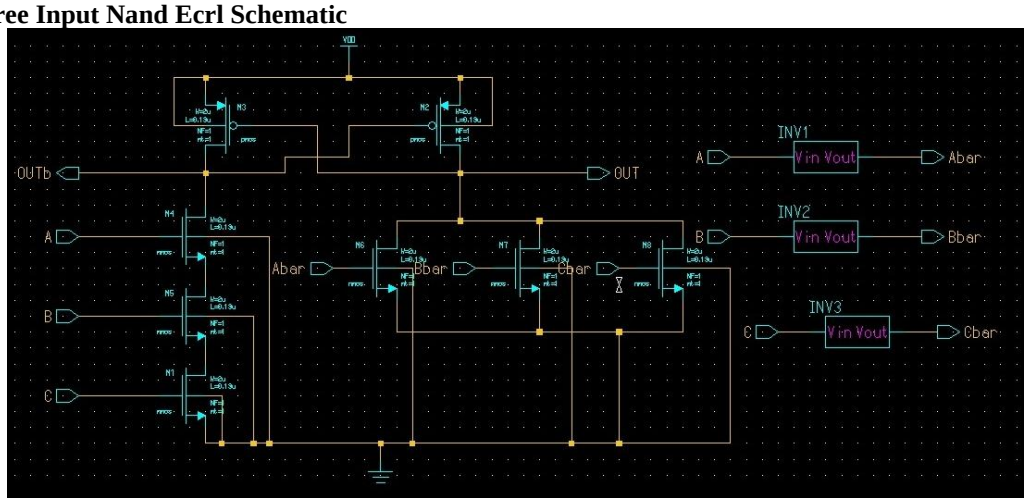

Fig. 4.1 NAND schematic

4.2 Simulated waveforms of Three input NAND

Fig 4.2 NAND waveforms

4.3 Universal 3 Input Nor Gate

The Boolean expression for 3 input NOR gate is Boolean Expression **Q = A+B+C**. It is implemented using ECRL logic with cross coupled PMOS transistors for recovery logic from node capacitances and parasitic capacitances.

4.4Three Input Nor Ecrl Schematic

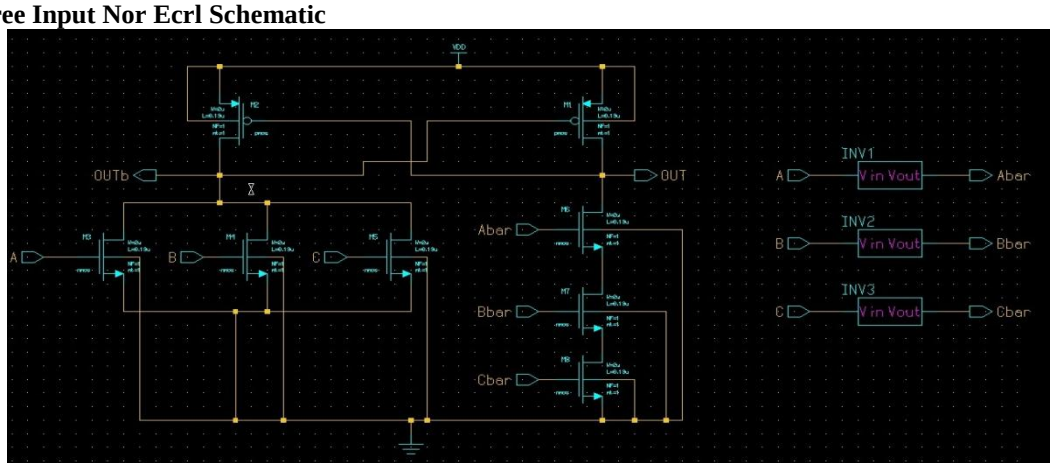

Fig. 4.4 NOR schematic

4.5 Three Input Nor Ecrl Waveforms

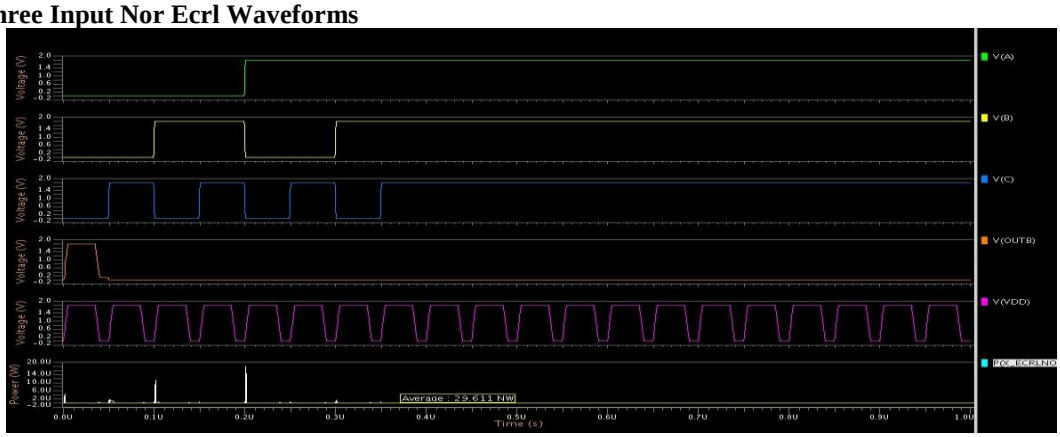

Fig. 4.5 Nor Waveforms

V. Design of Combinational Circuits

Combinational logic is used in computer circuits to perform Booleanalgebra on input signals and on stored data. Practical computer circuits normally contain a mixture of combinational and sequential logic. For example, the part of an arithmetic logic unit, or ALU, that does mathematical calculations is constructed using

combinational logic. Other circuits used in computers, such as half adders, full adders, half subtractors, full subtractors, multiplexers, demultiplexers, encoders and decoders are also made by using combinational logic.

5.1 Multiplexer

A multiplexer (or mux) is a device that selects one of several analog or digital input signals and forwards the selected input into a single line. A multiplexer of 2^n inputs has *n* select lines, which are used to select which input line to send to the output. Multiplexers are mainly used to increase the amount of data that can be sent over the network within a certain amount of time and bandwidth. A multiplexer is also called a data selector. Multiplexers can also be used to implement Boolean functions of multiple variables.

5.1.1Multiplexer Schematic

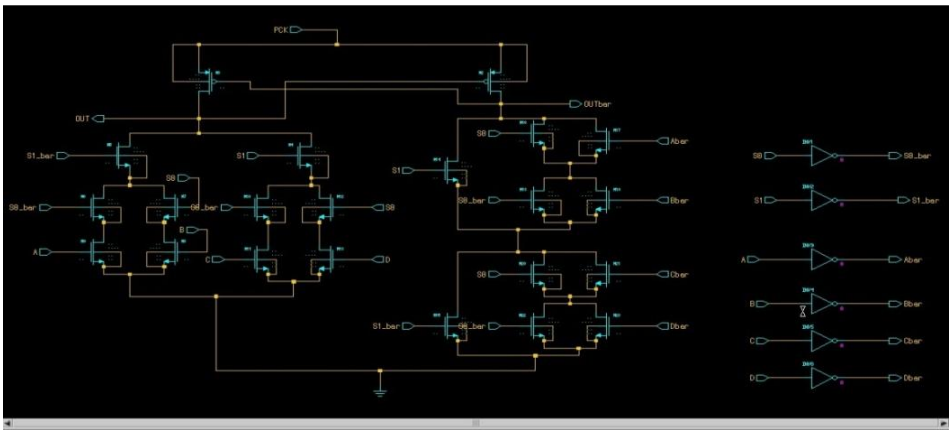

Fig. 5.1.1 Multiplexer Schematic

5.1.2 Multiplexer Output Waveforms

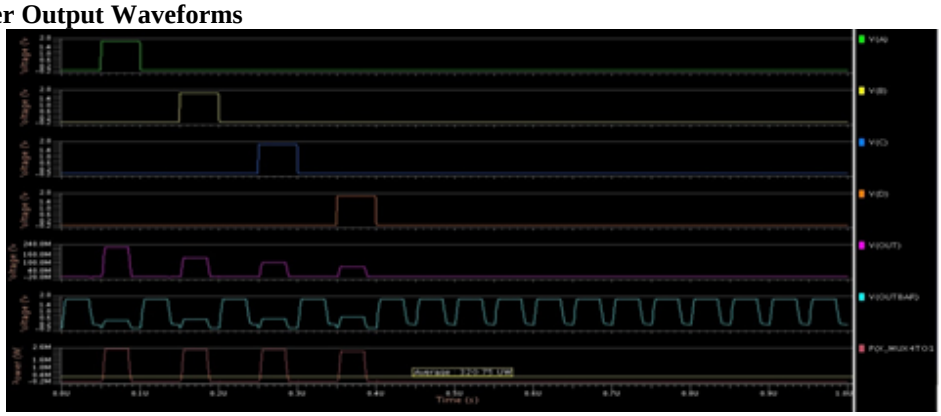

Fig. 5.1.2 Multiplexer waveforms

5.2 Decoder 2 By 4

A binary decoder is a combinational logic circuit that converts a binary integer value to an associated pattern of output bits. They are used in a wide variety of applications, including data DE multiplexing, seven segment displays, and memory address decoding.

5.2.1 Decoder Schematic with Power Efficient Adiabatic Nand Blocks

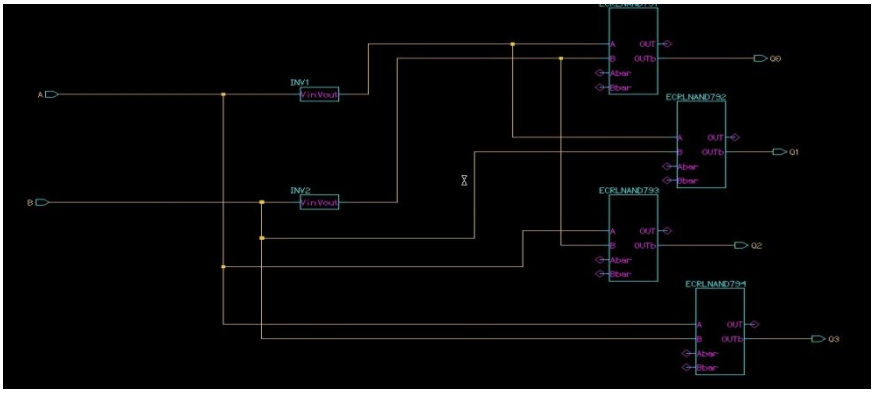

Fig. 5.2.1 Decoder schematic

5.2.2 Decoder Simulated Waveforms

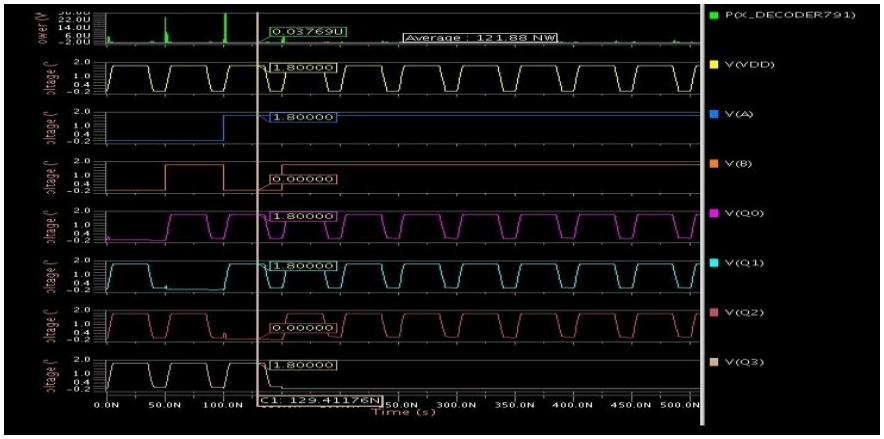

Fig. 5.2.2 Decoder waveforms

VI. Design of Sequential Circuit (D Flip Flop)

A flip-flop or latch is a circuit that has two stable states and can be used to store state information. A flip-flop is a bistablemultivibrator. The circuit can be made to change state by signals applied to one or more control inputs and will have one or two outputs. It is the basic storage element in sequential logic. Flip-flops and latches are fundamental building blocks of digital electronics systems used in computers, communications, and many other types of systems.

6.1 Edge Triggered D Flip Flop Schematic

The edge triggered flip flop changes states either at the positive edge(rising edge) or at the negative edge(falling edge) of the clock pulse on the control input.

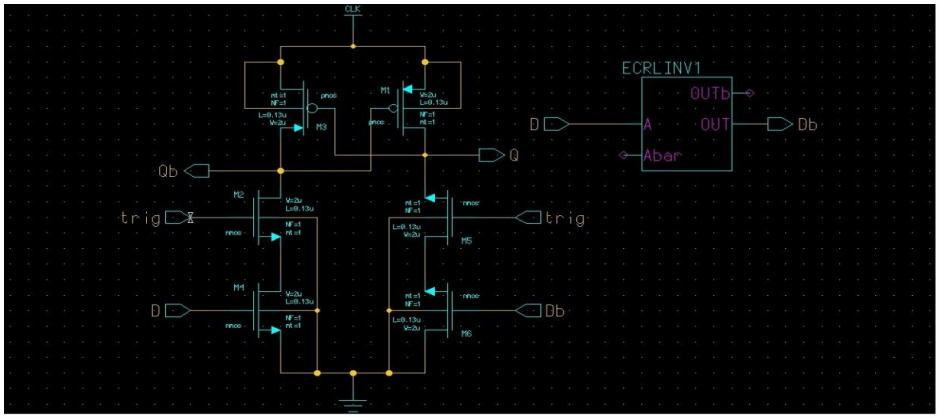

Fig. 6.1 Edge triggered D Flip Flop

6.2 D Flip Flop Simulated Waves

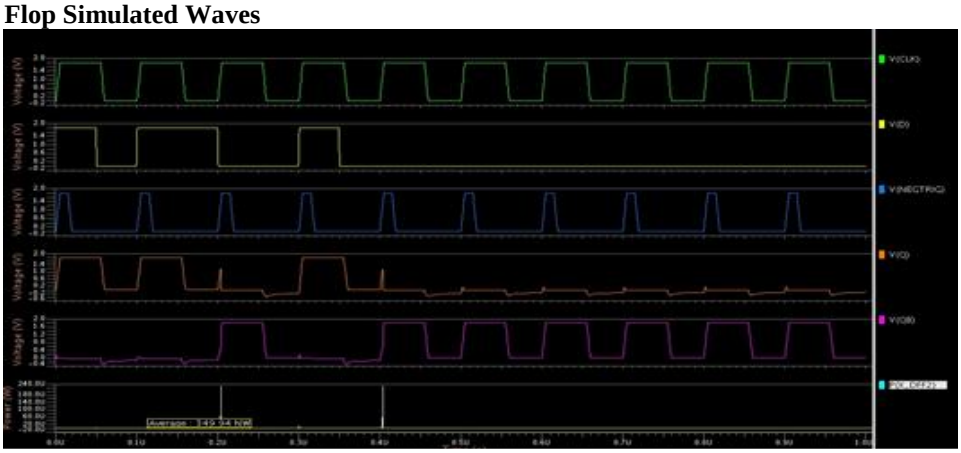

Fig. 6.2 D Flip Flop waveforms

VII. Comparison Table

CIRCUIT	CONVENTIONAL CIRCUITS		ADIABATIC LOGIC CIRCUITS	
	NO OF TRANSISTORS	AVERAGE POWER DISSIPATION	NO OF TRANSISTORS	AVERAGE POWER DISSIPATION
INVERTER	2	499.07nw	4	18.019nw
3 INPUT NAND	6	450.32nw	8	31.649nw
3 INPUT NOR	6	207.27nw	8	34.839nw
MULTIPLEXER	12	17.16mw[5]	10	320.73uw
DECODER	20	1.449uw	32	121.88nw
D FLIP FLOP	18	122.9uw[8]	8	349.94nw

Fig. 7 Comparison Table

VIII. Conclusion

This paper primarily focuses on lowering the power dissipation. Logics for invertor, universal gates, multiplexer, decoder and d Flip Flop are proposed and the results indicate that they have lesser power dissipation than some standard adiabatic logic styles. Their percentage power saving indicates their supremacy over conventional circuits. Moreover, in the proposed logic, the transistor count and the area per chip is also relatively lesser. The future scope of this work is that these blocks simulated can be used with higher number of input and output lines can be constructed by cascading the proposed blocks. The basics of adiabatic computation and the most well-known adiabatic logic families are described. However, new adiabatic design at high frequency may be targeted so that adiabatic circuit may be used in many high frequency applications also.

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